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09/266,869	03/12/1999	KAZUYA TANIGUCHI	P8075-9008	6342

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EXAMINER
PATEL, GAUTAM

ART UNIT	PAPER NUMBER
2653	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Application No.	Applicant(s)
09/266,869	Taniguchi et al.
Examiner	Art Unit
Gautam R. Patel	2653

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _three_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _May 8, 2002_

2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-23_ is/are pending in the applica

    4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-23_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some* c) ☐ None of:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    *See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____

DETAILED ACTION

1.   Claims 1-23 are pending for the examination. Claims 19-23 are newly presented for examination.

RCE STATUS

2.   The request filed on 10-9-01 for Request for continued Examination (RCE) under 37 CFR 1.114 based on parent Application is acceptable and a RCE has been established. An action on the RCE follows.

Claim Rejections - 35 U.S.C. § 112

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3.   Claims 1-18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
"Pseudo instruction" that is not executed required by the claims 1, ,8 14, 15 and 16 [preamble] is not described in the specification. On page 7, lines 1-3 the specification mentions "the pseudo is defined to be handled in the same manner as a no-operation (NOP) instruction by the instruction execution unit 12."; but does not explain at all that pseudo instruction is NOT executed. Accordingly, the specification does not explain to one of ordinary skill in the data processing "DP" art at the time of the invention, how to make and or use the invention comprising the claimed "pseudo instruction" that is not executed.
NOTE: It is well known in the art that no-operation instruction, or NOP, does NOT mean no-execution, it simply means when NOP is executed no operation takes place, hence name NOP. However nop-instruction does get executed.

4.
     The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 7, claims that "the pseudo instruction is not executed," [preamble] however same claim lines 11-12, claims that prefetching of instruction or data is taking place by execution of this instruction. This is confusing and unclear. It is not clear if instruction is executed or not.

Claims 8, 14, 15 and 16 has similar problems.

Claim Rejections - 35 U.S.C. § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

A person shall be entitled to a patent unless --
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, and 6-7 are rejected under 35 U.S.C. § 102(e) as being anticipated by Arora et al., US. patent 5,948,095 (hereafter Arora).

As to claim 1, Arora discloses the invention as claimed [see Figs. 1-3] including reading program from memory, detecting pseudo instruction and prefetching the instruction or data comprising the steps of:

a.   reading the program from the memory [col. 2, line 56 to col. 3, line 8];

b.   prefetching the instruction or data from the memory in accordance with the at least one instruction address or the data address [col. 3, lines 9-36 and col. 4, lines 17-31]; and

c.   storing the prefetched instruction or data in a buffer [col. 4, line 52 to col. 5, line 18; also see fig. 3, steps 300 and 305].

NOTE: the prefetch instruction of Arora works as a "pseudo instruction" of the applicants invention.

6.   As to claim 6, Arora discloses:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer when the pseudo instruction is detected [fig. 2 and col. 5, lines 43-67]; and

prefetching the instruction or data from the memory in accordance with the at least one instruction address or data address after the transfer of the at least one instruction to the first buffer has been identified [col. 4, lines 17-51].

7.   As to claim 7, Arora discloses:

Identifying that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected wherein the prefetch step is executed when the corresponding instruction or data is not stored in the second buffer [fig. 2 and col. 5, lines 43-67 and col. 4, lines 17-51].

8.   As to claims 15 and 22, they are rejected for the same reasons set forth in the rejection of claim 1, <u>supra</u>.

As to added limitation of the recording medium having program stored in them [see fig. 1, unit 103].

Claim Rejections - 35 U.S.C. § 103

9. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

10. Claims 2-5, 8-14, 16, 19-21 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arora as applied to claims 1, 6-7, 15 and 22 above.

11. As to claim 2, Arora discloses:

all of the above steps.

providing a pseudo instruction [prefetch instruction] detection unit [inherently present, when instructions are detected executed and data or instructions are retrieved form memory] connected with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the memory to the pseudo instruction detection unit with the buffer.

Arora does not teach that the buffer and detection units are connected in parallel. However it would have been obvious to a person of ordinary skill at the time of the invention to have placed the buffer and detection unit in parallel and put them into the system of Arora because doing so would make design more faster. As shown in "In re Japikse **86 USPQ 70 (CCPA 1950)**", to rearrange parts for different storage method is generally not given patentable weight or would have been obvious improvements.

12.   As to claim 3:

.   the buffer includes first and second buffers connected in parallel with the memory, and the method further comprising a step of storing, the instruction and data read from the memory in the first buffer and storing the prefetched instruction or data in the second buffer;

Arora does not teach additional instruction memories [or registers] or plurality of additional data memories. However it would have been obvious to a person of ordinary skill at the time of the invention to have combined additional instruction memories and additional data memories and put them into the system of Arora because doing so would make design more faster by storing these instructions and data in additional buffers. As shown in "St. Regis Paper Co. v Bemis Co. **193 USPQ 8 (7th Cir. 1977)**", to duplicate parts for multiple effects is generally not given patentable weight or would have been obvious improvements.

13.   As to claim 4, Arora discloses:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer when the pseudo instruction is detected [fig. 2 and col. 5, lines 43-67]; and

prefetching the instruction or data from the memory in accordance with the at least one instruction address or data address after the transfer of the at least one instruction to the first buffer has been identified [col. 4, lines 17-51].

14.   As to claim 5, Arora discloses:

Identifying that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected wherein the prefetch step is executed when the corresponding instruction or data is not stored in the second buffer [fig. 2 and col. 5, lines 43-67 and col. 4, lines 17-51].

15.   As to claim 8, Arora discloses:

a buffer [fig. 1, unit 121], connected to a memory [fig. 1, unit 103], for storing instructions and data of a program prefetched from the memory, wherein the program includes a pseudo instruction [prefetch instruction], at least one of an unconditional branch instruction [fig. 2, <branch>, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, and at least one instruction address or data address being part of the pseudo instruction [col. 5, lines 35-67];

an instruction execution unit [fig. 1, unit 100, which inherently has execution unit in it], connected to the buffer, for receiving the instruction and data from the buffer and executing a predetermined processing operation using the instruction and data [col. 5, lines 35-67].

a pseudo instruction detection unit [inherently present], connected to the memory [fig. 1, unit 103], for detecting the pseudo instruction included in the program prefetched from the memory;

an address control unit [inherently present], prefetching the instruction or data in accordance with at least one instruction address or data address when the pseudo instruction is detected [col. 4, lines 17-51].

16.   As to claim 9, it is rejected for the same reasons set forth in the rejection of
         claim 3, supra.

17.   As to claim 10, Arora discloses:

the address control unit identifies that the corresponding instruction or data is
stored in the second buffer in accordance with the at least one instruction address or
data address when the pseudo instruction is detected and permits storage of the
instruction or data in the second buffer when the corresponding instruction or data is
not stored in the second buffer [col. 3, line 37 to col. 4, line 31].

18.   As to claim 11, it is rejected for the same reasons set forth in the rejection of
claim 2, supra.

19.   As to claim 12, it is rejected for the same reasons set forth in the rejection of
claim 10, supra.

20.   As to claim 13, it is rejected for the same reasons set forth in the rejection of
claim 11, supra.

21.   As to claim 14, Arora discloses:

a detection circuit [inherently present], connected to a data line, for receiving the
pseudo instruction transferred on the data line and detecting the opcode included in the
pseudo instruction [col. 3, line 37 to col. 4, line 31]; as to the rest of the claim

Arora does not disclose a detection timing circuit, connected to the detection
circuit, for calculating instruction length or the number of operands of the pseudo
instruction from the opcode and determining the transfer period of the opcode based on
the instruction length or the number of operands, wherein the detection timing circuit
supplies a signal for validating the opcode detection operation during an operand
transfer period. "Official Notice" is taken that both the concept and the advantages of
providing a detection timing circuit which can calculate transfer period based on the
instruction length and number of operands are well known. It would have been obvious

to provide a timing circuit to Arora' system as this circuit is known to provide the system with a timing estimate and send valid operand into the system. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

22.   As to claim 16, it is rejected for the same reasons set forth in the rejection of
       claim 1 and 8, supra.
       As to the added limitation of
       a bus interconnecting the prefetch buffer and the memory [inherently present].

23.   As to claims 19-21 and 23, they are claims corresponding to claims 1, 8, 14 and
       16 respectively and they are therefore rejected for the same reasons set forth in
       the rejection of claims , 8, 14 and 16 in paragraph respectively, supra.

Allowable Subject Matter

24.   Claims 17 and 18 are objected as being dependent upon a rejected base claim,
       but would be allowable if rewritten in independent form including all of the
       limitations of the base claim and any intervening claims; and subject to
       overcoming 112 first and second rejection supra.

25.   Applicant's arguments with respect to claims 1-23 have been considered but are
       deemed to be moot in view of the new grounds of rejection.

Other prior art cited

26.   The prior art made of record and not relied upon is considered pertinent to
       applicant's disclosure.

a.   Tirumalai et al. (US. patent 6,341,370) "Integration of data prefetching and modulo scheduling using postpass prefetch insertion".

b.   Santhanam (US. patent 5,704,053) "Efficient explicit data prefetching analysis and code generation in a low level optimizer for inserting prefetch instructions into loops of applications."

Contact information

27.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.
The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is (703) 872-9314.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. William Korzuch, can be reached on (703) 305-6137.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-4700 or the group Customer Service section whose telephone number is (703) 306-0377.

RICHARD L. ELLIS
PRIMARY EXAMINER

Gautam R. Patel
Patent Examiner
Group Art Unit 2653

June 1, 2002